

09/976523

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ISSUE CLASSIFICATION	
Class	Subclass

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PATENT NUMBER

U.S. **UTILITY** Patent Application

122 O.I.P.E. 1
SCANNED Q.A. 1c

PATENT DATE

APPLICATION NO. 09/976523	CONT/PRIOR	CLASS 324 718	SUBCLASS 725	ART UNIT -2858 2133	EXAMINER Dorado
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APPLICANTS

Michael Dorsey

TITLE

Utilizing slow ASIC logic BIST to preserve timing integrity across timing domains

PTO-2040
12/99

ISSUING CLASSIFICATION

[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)		NOTICE OF ALLOWANCE MAILED _____	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	_____ (Primary Examiner)		ISSUE FEE	
	_____ (Date)		Amount Due .	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)		ISSUE BATCH NUMBER _____	
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